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for a limited area numerical weather forecast routine
Robert van Engelen , Lex Wolters
Proceedings of the 9th international conference on Supercomputing July 1995

- 2 Performance of the CRAY T3E multiprocessor 95%
Ed Anderson , Jeff Brooks , Charles Grassl , Steve Scott
Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM)
November 1997

The CRAY T3E is a scalable shared-memory multiprocessor based on the DEC Alpha 21164 microprocessor. The system includes a number of novel architectural features designed to tolerate latency, enhance scalability, and deliver high performance on scientific and engineering codes. Included among these are **stream buffers**, which detect and prefetch down small-stride reference streams, **E-registers**, which provide latency hiding and non-unit-stride access capabilities, barrier and fetch_an ...

- 3 Compiler transformations for high-performance computing 94%
David F. Bacon , Susan L. Graham , Oliver J. Sharp
ACM Computing Surveys (CSUR) December 1994
Volume 26 Issue 4

In the last three decades a large number of compiler transformations for optimizing programs have been implemented. Most optimizations for uniprocessors reduce the number of instructions executed by the program using transformations based on the analysis of scalar quantities and data-flow techniques. In contrast, optimizations for high-performance superscalar, vector, and parallel processors maximize parallelism and memory locality with transformations that rely on tracking the properties o ...


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 ... set when it is necessary to **invalidate** cache. ... 5 of 39 "cpu" command to **disable**

 instruction buffer ... On non-cached **Cray vector** systems, performance on **vector** ...

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 ... can't do this for a **vector** processor ... Challenge shared memory bus <= 32 1 **Cray T3D**

 shared ... cache • two kinds of protocols • **invalidate** protocol: **invalidate** ...

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 ... Machines • Scalable machines, like **CRAY T3E**, **disable** ... 2. Home clears presence **vector**,

 presence[requestor ... The number of transactions to **invalidate** sharers is ...

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 ... Process Control Block), Interrupt **vector** register — Stack ... duration —Conditional

 branch instruction — **Invalidate** several instruction ... Used in CDC and **CRAY-1** ...

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 ... The applications run under the full-map, write-**invalidate** Stache coherence protocol

 with 32 ... (We currently do not support the CM-5 **vector** units.). ... **CRAY T3D**: A New. ...

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 ... 1 Except in the case of the **Cray**, which does ... operations over large aggregate data

 structures such as **vectors**. ... Munin, DASH uses a write **invalidate** protocol for ...

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 ... to take into account the **Cray** specificities, the ... dependence rules would suggest

 to **invalidate** the resource ... C library that handles **vectors**, matrices, linear ...

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